IN THE SPECIFICATION

Please amend paragraph [0002] as follows:

[0002] Digital data is often stored by being electronically "written" to the surface of a disk in a hard-disk drive. This digital data or information is retrieved, or read back, by means of a magneto-resistive ("MR") element in close proximity to the spinning disk. The small signal (in the millivolt range) from the MR element in a hard disk drive must be AC-coupled before it is presented to the reader amplifier due to the significant DC voltage (up to several hundred millivolts) across the MR element. The low-corner -3dB frequency of that AC coupling must be set low enough so that none of the significant bandwidth of the signal is lost. Low-corner -3dB frequencies ~~in~~ on the order of 1 MHz and above are conventionally available. However, recent advances in disk drive technology such as vertical recording, have required that the low-corner -3dB frequency be lowered by around an order of magnitude. This is significant enough to require modifications to the design of the reader amplifier front-end. The reader amplifier input stage has traditionally been comprised of NPN bipolar transistors because of their low noise characteristics. However, the base current associated with these transistors makes it difficult to achieve the low-corner -3dB frequency required for vertical recording.

Please amend paragraph [0014] as follows:

[0014] The transconductance of an all-bipolar junction transistor pair can be set by a predetermined tail current. However, the transconductance of a bipolar/MOS differential pair is not set by a predetermined tail current as is the case with an all-bipolar pair. Thus it is an objective of the present invention to configure an input stage using both a bipolar transistor, such as an NPN, coupled to the MR element and an MOS transistor, such as and NMOS (which has no input current equivalent to the bipolar NPN's base current) coupled to the AC-coupling capacitor. Alternatively, PNP and PMOS transistors can be used to accomplish the objectives of the present invention assuming a reversal of the polarity of the corresponding circuit. Although, a single bipolar/MOS differential pair is described herein, such description is not meant to be limiting as a plurality of bipolar and MOS transistors arranged as differential pairs can be used to implement the present invention.

Please amend paragraph [0016] as follows:

[0016] It is well-known in the art to use a scaled master stage with a given offset. However, the novel aspect of the present invention is that the scaled master stage with a given offset is preceded by a balanced stage to ~~determine~~ provide the scaled master stage with a balanced offset. It is desirous to have an input stage differential pair designed with an NPN and an NMOS device, or PNP and PMOS device, in order to achieve a low, low-corner –3dB frequency as well as low noise. As noted, conventional arrangements that use bipolar transistors as the input differential pair allow the gain to be accurately determined from the tail current as bipolar transconductance is set precisely by the current. However, there are significant advantages to using a MOS transistor as one of the differential pair devices. Disadvantageously, gain cannot be set by a predetermined tail current when a MOS transistor as one of the differential pair devices. In such case, a feedback means is needed to set the tail current of the differential pair to achieve the desired gain.